Atty. Dkt. No. 039153-0223 (E0554)

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-17 (Cancelled)

18. (Original) An integrated circuit including a plurality of field effect transistors, each of the transistors comprising:

a gate structure disposed over a channel;

a deep source region heavily doped with dopants of a first conductivity type;

a deep drain region heavily doped with dopants of the first conductivity type;

a source extension integral the deep source region; and

a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension.

19. (Re-presented – Formerly Dependent Claim #19) ~~The integrated circuit of claim 18,~~ An integrated circuit including a plurality of field effect transistors, each of the transistors comprising:

a gate structure disposed over a channel;

a deep source region heavily doped with dopants of a first conductivity type;

a deep drain region heavily doped with dopants of the first conductivity type;

a source extension integral the deep source region; and

a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension wherein the source extension is more heavily doped than the drain extension.

20. (Original) The integrated circuit of claim of claim 19, wherein the drain extension is more than 80 nm thick and the source extension is less than 40 nm thick.

21. (Previously Added) An integrated circuit includes a gate structure disposed over a channel, a deep source region heavily doped with dopants of a first conductivity type, a deep drain region heavily doped with dopants of the first conductivity type, a source extension integral the deep source region, and a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension, wherein the integrated circuit is manufactured by a method, comprising:

providing the gate structure between a source location and a drain location in a semiconductor substrate;

providing an angled source extension implant in a direction from the source location to the drain location;

providing an angled drain extension implant in a direction from the drain location to the source location; and

providing a deep source/drain implant at the source location and the drain location.

22. (Previously Added) The integrated circuit of claim 21, further comprising providing a pair of spacers abutting lateral sides of the gate structure before the deep source drain implant.

23. (Previously Added) The integrated circuit of claim 22, wherein the providing the source extension step is a low energy, high dose ion implantation step.

24. (Previously Added) The integrated circuit of claim 23, wherein the drain extension implant step is a medium energy, high dose ion implantation step.

25. (Currently Amended) The integrated circuit of claim 24, wherein a the source extension formed by the source extension step is shallower than a the drain extension formed by the drain extension implant step.

26. (Previously Added) The integrated circuit of claim 25, wherein the source extension has approximately 5 times the concentration of dopants of the drain extension.

27. (Previously Added) The integrated circuit of claim 25, wherein the source extension has a concentration of $5x10^{19}$-$1x10^{20}$ of dopants per centimeter cubed and the drain extension has a concentration of $1x10^{19}$-$5x10^{19}$ dopants per centimeter cubed.

28. (Previously Added) The integrated circuit of claim 25, wherein the drain extension has a concentration between $1x10^{19}$ - $5x10^{19}$ dopants per centimeter cubed.

29. (Previously Added) The integrated circuit of claim 25, wherein the drain extension is more than 80 nm deep.

30. (Previously Added) The integrated circuit of claim 27, wherein the gate structure is associated with a N-channel or P-channel with MOSFET.

31. (Previously Amended) An ultra-large scale integrated circuit including a plurality of field effect transistors, the field effect transistors comprising:

a gate structure on a top surface of a semiconductor substrate;

a source extension with dopants of a first conductivity type;

a drain extension with dopants of the first conductivity type; and

deep source and drain regions with dopants of the first conductivity type, wherein the gate structure is between the source and drain regions, wherein the drain extension is deeper than the source extension.

32. (Previously Amended) The integrated circuit of claim 31, further comprising:

a pair of spacers abutting lateral sides of the gate structure.

33. (Previously Added) The integrated circuit of claim 31, wherein the drain extension is formed in a low dosage implant process.

34. (Previously Added) The integrated circuit of claim 31, wherein the source extension is formed at an energy level of between 1-5 KeV.

35. (Previously Added) The integrated circuit of claim 31, wherein the drain extension is formed at an energy level of between 5-15 KeV.

36. (Previously Amended) The integrated circuit of claim 31, wherein the deep source and deep drain regions have a concentration of dopants between 10^{19} and 10^{20} dopants per cc, the source extension has a concentration of dopants between $5X10^{19}$ and 10^{20} dopants per cc, and the drain extension has a concentration of dopants between $1X10^{19}$ and $5X10^{19}$ dopants.

37. (Previously Amended) The integrated circuit of claim 31, wherein the first conductivity type is P-type or N-type.